

Topic 3: Controlling the Computer

Assembling the Components
Reference : Handout

Get Microcode emulator from here:
<http://info.comp.lancs.ac.uk/year1/notes/csc131/>

C.Sc. 131: Systems Architecture - 2006

The Key Components

- Flip-flops, grouped together to form fixed size registers.
- Adders, grouped together to operate on fixed size numbers.
- A section of main memory.
- I/O devices.
- Design decision: the word size of our computer.

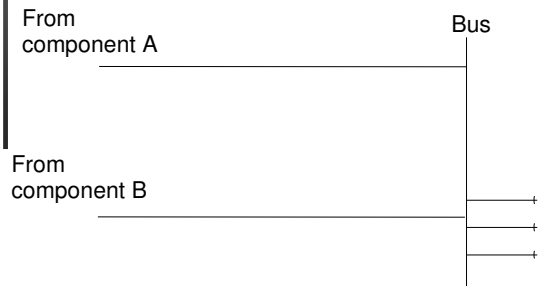
C.Sc. 131: Systems Architecture - 2006

Data Buses

- Need to be able to move information between the components.
- Data Buses: a collection of wires which connect together the components.
- Width of the bus is normally equal to the word size.
- Access to the bus is controlled by placing AND and OR gates between each component and the bus.

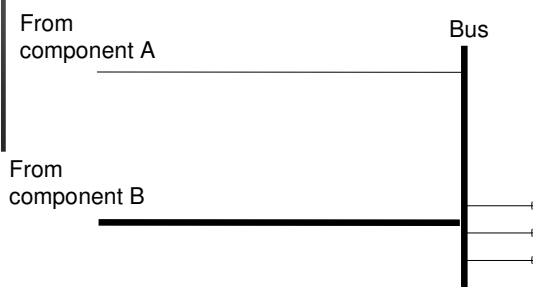
C.Sc. 131: Systems Architecture - 2006

Data Buses ... contd.



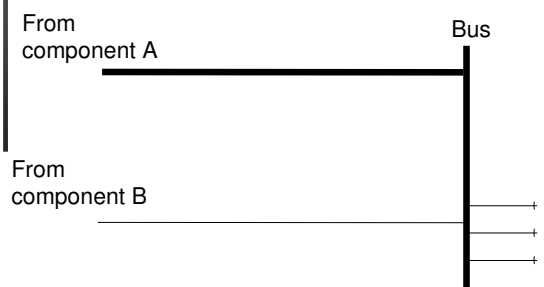
C.Sc. 131: Systems Architecture - 2006

Data Buses ... contd.

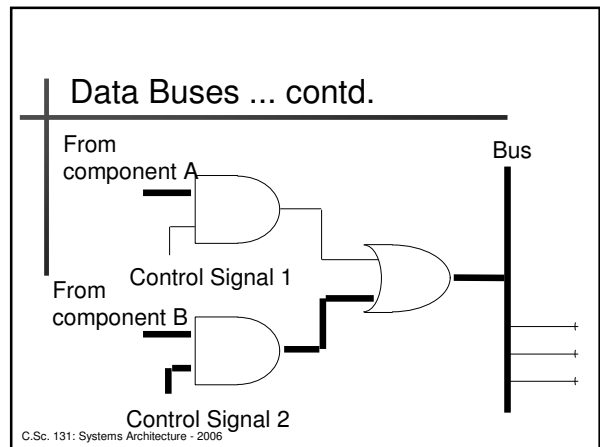
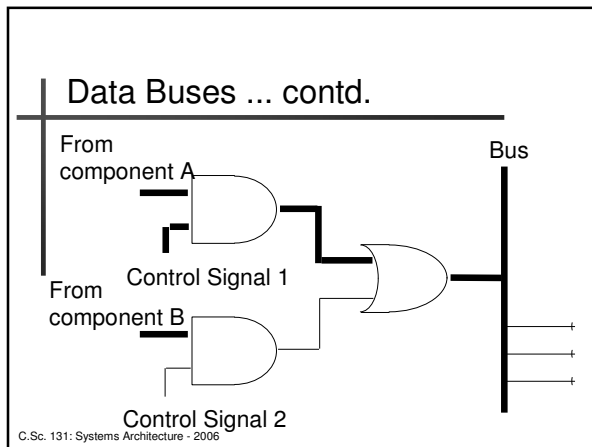
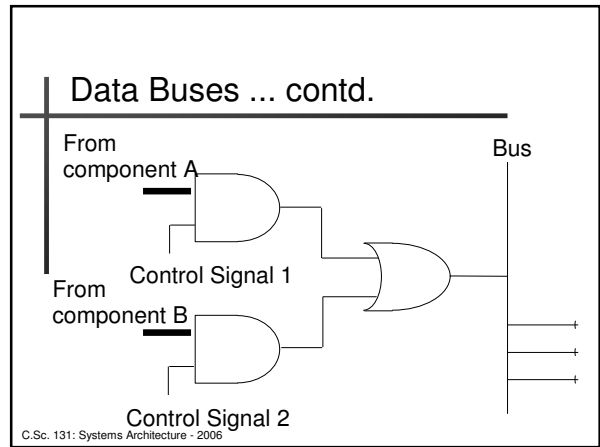
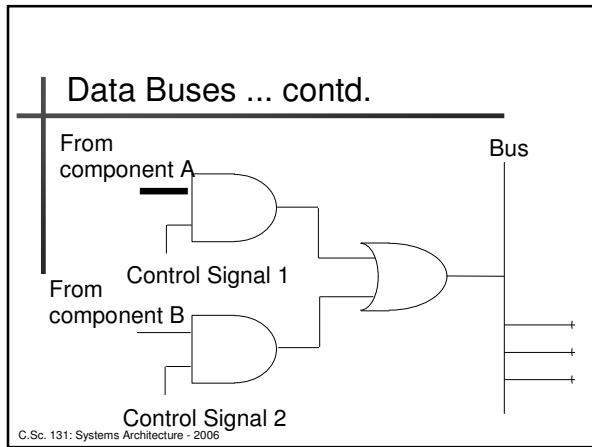
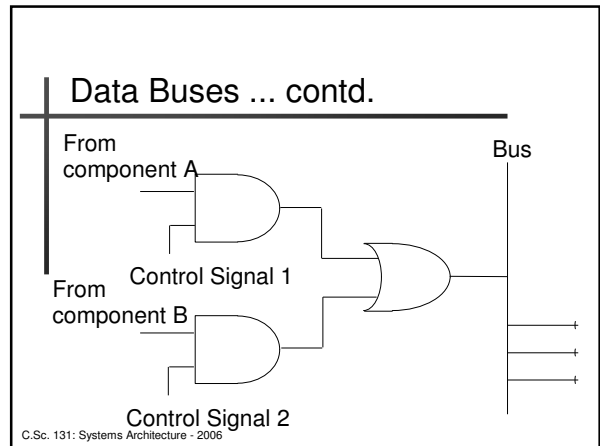
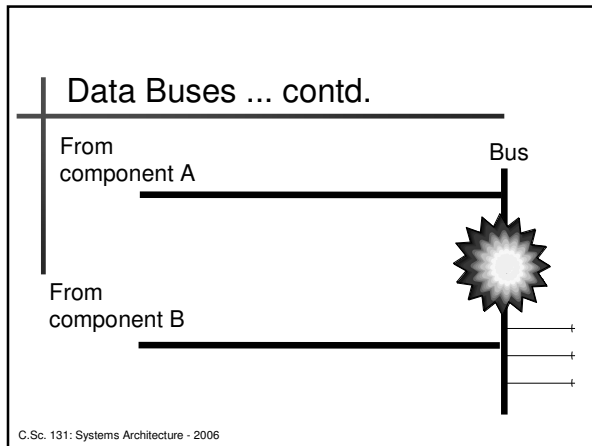


C.Sc. 131: Systems Architecture - 2006

Data Buses ... contd.



C.Sc. 131: Systems Architecture - 2006



Control Logic

- Many of the components need control signals to regulate their activity.
- Control signals are produced by a computer component called the control logic.
- The control logic incorporates a clock which produces signals at a regular rate.
- Clock signals are used to synchronise the components.

C.Sc. 131: Systems Architecture - 2006

A Stored Program Computer

C.Sc. 131: Systems Architecture - 2006

Features: Registers and Buses

- 8 Registers
 - A, B, C and D General purpose
 - MPC Microprogram counter
 - MIR Microinstruction register
 - MDR Memory data register
 - MAR Memory address register
- Data in the registers can be transferred onto the buses using control signals.

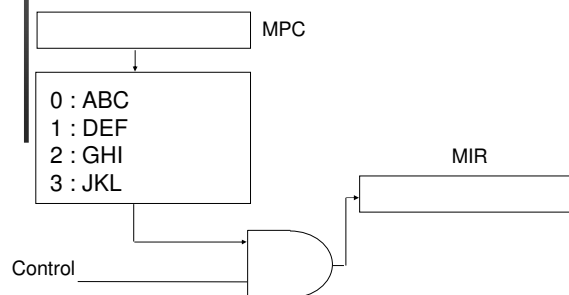
C.Sc. 131: Systems Architecture - 2006

Features : Micro memory (1)

- Each cell contains 22 bits, cells addressed as 0 .. 1023.
- Contents of micro memory can be accessed by placing a valid address in the MPC register.
- The value at this address is copied into the MIR on the appropriate signal.

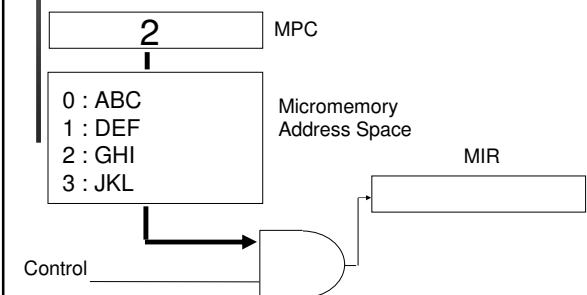
C.Sc. 131: Systems Architecture - 2006

Features: Micro memory



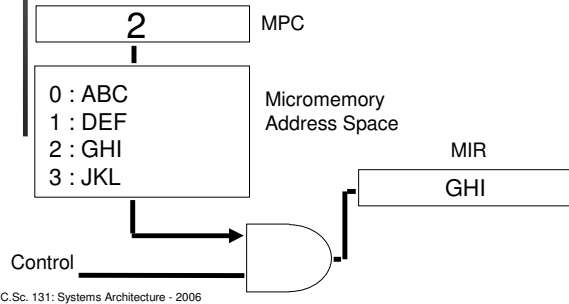
C.Sc. 131: Systems Architecture - 2006

Features: Micro memory



C.Sc. 131: Systems Architecture - 2006

Features: Micromemory



Features: Main Memory

- Each cell contains 16 bits, cells addressed as 0 .. 4095
- Contents of main memory can be accessed by placing a valid address in the MAR.
- If control signal 15 is set then the value held at this address is copied into the MDR.
- If control signal 16 is set then the value held in the MDR is copied into the memory at this address.

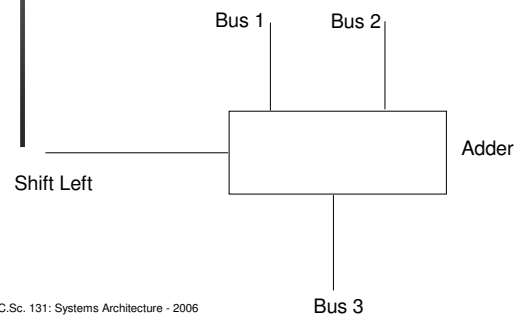
C.Sc. 131: Systems Architecture - 2006

Features of Our Computer: The Adder

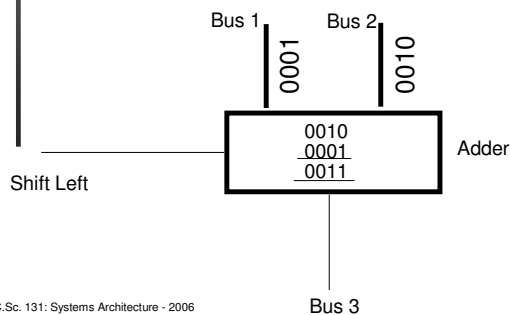
- The adder performs arithmetic on the values on BUS1 and BUS2 and places the result on BUS3.
- Setting control signal 7 causes the adder to perform a subtraction rather than an addition.
- If control signal 8 is set the adder shifts the result of its arithmetic (multiplies by 2).

C.Sc. 131: Systems Architecture - 2006

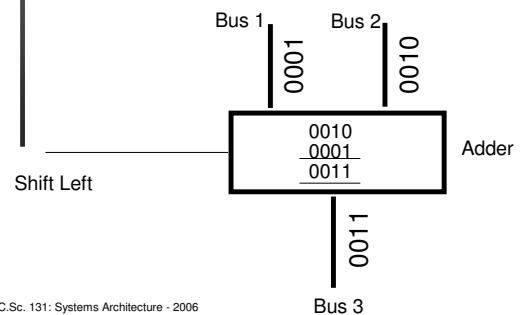
Features: The Adder



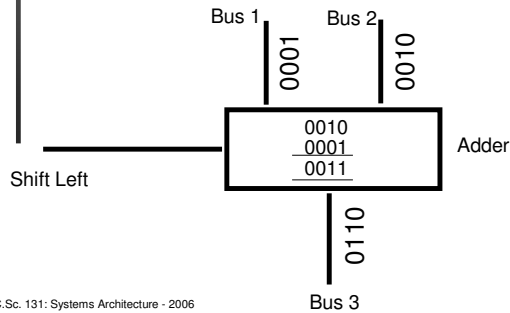
Features: The Adder



Features: The Adder



Features: The Adder



C.Sc. 131: Systems Architecture - 2006

Features: Test, Signals and Others

- Machine can perform two tests:
 - Test if register A contains zero.
 - Test if the MSB of A is set.
- Control signals 5 and 17 place a 1 on BUS2.
- Control signal 21 places the 4 most significant bits of the MDR onto BUS2.
- Control signal 18 places the 10 most significant bits of the MIR onto BUS2.

C.Sc. 131: Systems Architecture - 2006

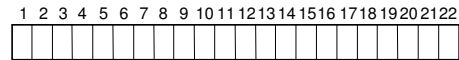
Programming Our Computer

- The behaviour of our computer depends entirely on the values of the control signals.
- Question: what causes the signals to be turned on and off ?

C.Sc. 131: Systems Architecture - 2006

Programming Our Computer

- The behaviour of our computer depends entirely on the values of the control signals.
- Question: what causes the signals to be turned on and off ?
- Answer: the register MIR contains a microinstruction which specifies which lines are to be switched on.



C.Sc. 131: Systems Architecture - 2006

Regulating the Control Signals

- Consider if bits 2, 5 and 10 are set.
- The effect should be to add 1 to the contents of B.
- The control signals which may be turned on at any point in time are regulated by a clock.
- Each microinstruction takes one clock cycle to execute.
- Each cycle is broken down into 5 phases, during each phase only certain signals may be on.

C.Sc. 131: Systems Architecture - 2006

The Phases of the Clock

Clock Phase	Control signals which may be turned on
1	1 - 8
2	9 - 14
3	15 - 16
4	17 - 22
5	control signals marked 'PHASE 5'

- Now consider if bits 2, 5 and 10 are set.
- Note that the MIR contains the instruction currently being executed and MPC contains the memory address of this instruction.

C.Sc. 131: Systems Architecture - 2006

A Sample Micro program

- A sample micro program to multiple the contents of register C by register A.
- Results are placed in main memory cell 1.

```

module multiply
{
  set MDR to 0
  repeat A times
    add C to MDR
  move 1 to MAR and tell the main memory to write
}
    
```

C.Sc. 131: Systems Architecture - 2006

Sketch of the Microprogram

Micromemory address	Microinstruction
0	0 + 0 -> MDR; MPC + 1 -> MPC;
1	MPC + TESTZERO(A) -> MPC
2	5 -> MPC
3	C + MDR -> MDR; MPC + 1 -> MPC;
4	A - 1 -> A; 0 + 1 -> MPC
5	0 + 1 -> MAR; write; MPC + 1 -> MPC

C.Sc. 131: Systems Architecture - 2006

The Microprogram in Full

Micromemory address	Microinstruction																					
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
0																						
1																						
2																						
3																						
4																						
5																						

C.Sc. 131: Systems Architecture - 2006

The Microprogram in Full

Micromemory address	Microinstruction																					
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
0																						
1																						
2																						
3																						
4																						
5																						

C.Sc. 131: Systems Architecture - 2006

The Microprogram in Full

Micromemory address	Microinstruction																					
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
0																						
1																						
2																						
3																						
4																						
5																						

C.Sc. 131: Systems Architecture - 2006

The Microprogram in Full

Micromemory address	Microinstruction																					
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
0																						
1																						
2																						
3																						
4																						
5																						

C.Sc. 131: Systems Architecture - 2006

The Microprogram in Full

		Microinstruction																					
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Micromemory address	0															1			1				1
	1																			1			1
	2							1		1									1				
	3			1			1							1					1				1
	4	1			1		1		1										1				
	5					1									1		1	1					

C.Sc. 131: Systems Architecture - 2006

Phase 5

C.Sc. 131: Systems Architecture - 2006

Summary

- The behaviour of a computer depends on the values of various control lines and the state of the computer's clock.
- The values that the control lines take are specified as microinstructions.
- The microinstructions are stored in special memory called micromemory.

C.Sc. 131: Systems Architecture - 2006

Coming Next Week

- Evaluation of microinstructions.
- Using machinelanguage to provide programmers with an easier interface to our computer.
- Reference : D & L pp 199-215

C.Sc. 131: Systems Architecture - 2006